

IN THE CLAIMS

Below, please find a clean, unmarked copy of the claims. Please amend claim 10.

Claims 1-9 and 11-19 are re-presented.

- 1 1. A method of forming a transistor, comprising:
2 forming an alignment component on a substrate of a semiconductor material, said
3 alignment component consisting of a single material;
4 depositing a metal layer over the substrate and the alignment component;
5 reacting the metal layer with the semiconductor material of the substrate to form two
6 silicide regions, the silicide regions having inner surfaces which face one another, wherein an
7 upper portion of each inner surface contacts the alignment component and a lower portion of
8 each inner surface contacts the semiconductor material of the substrate;
9 removing the alignment component; and
10 replacing the removed alignment component with a conductive gate.
- 1 2. The method of claim 1 wherein the alignment component is non-conductive.
- 1 3. The method of claim 2 wherein the alignment component is made of a material
2 selected from the group consisting of a silicon oxide and silicon nitride.
- 1 4. The method of claim 1 wherein the alignment component is made of a material which
2 does not react with the metal layer when the metal layer is reacted with the semiconductor
3 material of the substrate.

1 5. The method of claim 1 wherein the alignment component has a thickness of between
2 1000Å and 2500Å.

1 6. The method of claim 1 wherein the alignment component is less than 0.10 microns
2 wide.

1 7. The method of claim 1 wherein the metal layer is selected from the group consisting of
2 a material comprising tungsten, cobalt and titanium.

1 8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å thick.

1 9. The method of claim 1 wherein the silicide regions have lower surfaces located lower
2 than a lower surface of the alignment component.

Amended
1 10. (Three Times Amended) The method of claim 1 wherein removing the alignment
2 component comprises:
3 depositing a layer over the silicide regions and the alignment component;
4 planarizing the layer at least until the alignment component is exposed; and
5 etching the alignment component at least until the substrate is exposed to leave an
6 opening between the inner surfaces of the silicide regions to allow for formation of the
7 gate.

1 11. The method of claim 10 wherein, after the etching of the alignment component, the
2 upper portions of the inner surfaces are exposed.

1 12. The method of claim 10 wherein the alignment component and the layer are made of
2 different materials, one being made of a silicon oxide and the other being made of silicon
3 nitride.

1 13. The method of claim 1 wherein the gate is formed according to a method comprising:
2 depositing a gate dielectric layer; and
3 forming a gate electrode on the gate dielectric layer.

1 14. The method of claim 13 wherein the gate dielectric layer is less than 10Å thick.

1 15. The method of claim 13 wherein the gate electrode is made out of a metal.

1 16. The method of claim 1, further comprising:
2 forming doped regions which extend from the silicide regions in underneath the gate.

1 17. The method of claim 13 wherein the gate dielectric layer has a dielectric constant of at
2 least 100.

1 18. The method of claim 13 wherein the gate dielectric layer comprises a material selected
2 from the group consisting of strontium titanate, and barium strontium titanate.

1 19. The method of claim 17 wherein the gate electrode comprises a material selected from
2 the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.